IN THE CLAIMS:

1. (Currently Amended) A pipeline structure for use in a digital system, said pipeline structure comprising:

a plurality of stages arranged in a sequence from a first stage for receiving an input of the pipeline structure to a last stage for providing an output of the pipeline structure, with at least two ~~one~~ intermediate stages ~~stage~~ being interposed between the first stage and the last stage; and

a phase shifting circuit for generating at least two ~~one~~ local clock signals ~~signal~~ each for controlling a corresponding one of the at least two ~~one~~ intermediate stages ~~stage~~,

wherein for each of the intermediate stages, the phase shifting circuit includes a delay block for producing the local clock signal controlling that intermediate stage from the clock signal controlling a next one of the stages in the sequence,

the first stage and the last stage are controlled by a main clock signal,

the at least two ~~one~~ local clock signals are ~~signal is~~ generated from the main clock signal, and

the main clock signal and the at least two ~~one~~ local clock signals ~~signal~~ are out of phase with one another.

2-4. (Canceled)

5. (Currently Amended) The pipeline structure according to claim 1 [[4]], wherein each of the intermediate stages includes a functional unit cascade connected to a buffer, the buffer storing an output of the functional unit of a previous one of the stages in the sequence based on the corresponding local clock signal, and the functional unit having a propagation time that is less than a phase difference between the corresponding local clock signal and the clock signal controlling the next one of the stages in the sequence.

6. (Original) The pipeline structure according to claim 5, wherein each of the functional units consists of a combinatorial circuit and each of the buffers consists of a register for storing a word.

7. (Original) The pipeline structure according to claim 1, wherein for each of the at least one intermediate stages, the phase shifting circuit includes a delay block for producing the local clock signal controlling that intermediate stage from the clock signal controlling one of the stages that is adjacent in the sequence.

8. (Currently Amended) A digital system including at least one pipeline structure, the pipeline structure comprising:

a plurality of stages arranged in a sequence from a first stage for receiving an input of the pipeline structure to a last stage for providing an output of the pipeline structure, with at least two ~~one~~ intermediate stages ~~stage~~ being interposed between the first stage and the last stage; and

a phase shifting circuit for generating at least two ~~one~~ local clock signals ~~signal~~ each for controlling a corresponding one of the at least two ~~one~~ intermediate stages ~~stage~~,

wherein for each of the intermediate stages, the phase shifting circuit includes a delay block for producing the local clock signal controlling that intermediate stage from the clock signal controlling a next one of the stages in the sequence,

the first stage and the last stage are controlled by a main clock signal,

the at least two ~~one~~ local clock signals are ~~signal is~~ generated from the main clock signal, and

the main clock signal and the at least two ~~one~~ local clock signals ~~signal~~ are out of phase with one another.

9-11. (Canceled)

12. (Original) The digital system according to claim 8, wherein the digital system is a synchronous digital system.

13. (Original) The digital system according to claim 8, wherein the digital system is a controller or microprocessor integrated in a chip.

14. (Currently Amended) An electronic device comprising:

a digital system including at least one pipeline structure, the pipeline structure including:

a battery for supplying power to the digital system;

a plurality of stages arranged in a sequence from a first stage for receiving an input of the pipeline structure to a last stage for providing an output of the pipeline structure, with at least two ~~one~~ intermediate stages ~~stage~~ being interposed between the first stage and the last stage, and the first stage and the last stage being controlled by a main clock signal; and

a phase shifting circuit for generating at least two ~~one~~ local clock signals ~~signal~~ each for controlling a corresponding one of the at least two ~~one~~ intermediate stages ~~stage~~, the at least two ~~one~~ local clock signals ~~signal~~ being generated from the main clock signal, and the main clock signal and the at least two ~~one~~ local clock signals ~~signal~~ being out of phase,

wherein for each of the intermediate stages, the phase shifting circuit includes a delay block for producing the local clock signal controlling that intermediate stage from the clock signal controlling a next one of the stages in the sequence~~; and~~

~~a battery for supplying the digital system~~.

15-17. (Canceled)

18. (Original) The electronic device according to claim 14, wherein the electronic device is a hand-held computer and the digital system is a controller or microprocessor of the hand-held computer.

19. (Currently Amended) A method of operating a pipeline structure that includes a plurality of stages arranged in a sequence from a first stage for receiving an input of the pipeline structure to a last stage for providing an output of the pipeline structure, with at least two ~~one~~ intermediate stages ~~stage~~ being interposed between the first stage and the last stage, said method comprising the steps of:

controlling the first stage and the last stage with a main clock signal;

generating, with a delay block, at least two ~~one~~ local clock signals ~~signal~~ from the main clock signal, the main clock signal and the at least two ~~one~~ local clock signals ~~signal~~ being out of phase; and

controlling each of the at least two ~~one~~ intermediate stages ~~stage~~ with a different one of the at least two ~~one~~ local clock signals ~~signal~~, wherein each of the local clock signals is out of phase with the other and is produced from a next one of the stages in the sequence.

20-22. (Canceled)

23. (Currently Amended) The method according to claim 19 [[22]], wherein in the generating step, the local clock signal for each of the intermediate stages is generated from the clock signal controlling a next one of the stages in the sequence.